

Exhibit 2

A HIGH-EFFICIENCY 1.5 kW, 390-50 V HALF-BRIDGE CONVERTER OPERATED AT 100% DUTY-RATIO

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ABSTRACT — A half-bridge isolated step-down converter operated at nearly unity duty-ratio for very high efficiency is discussed. It is meant to interface the 390 V regulated output of a 1.5 kW power factor correction unit to a 50 V distribution bus. It is based on the zero-voltage switching scheme of the phase-shifted PWM approach, but since the duty ratio does not vary from near unity, the output inductor is omitted. The ring of the output rectifier capacitance with the transformer leakage inductance is therefore clamped by the output capacitor, which permits the oscillation energy to be recovered. This, together with zero-voltage switching of the MOSFETs, gives the converter an efficiency greater than 95% at full load.

Distributed Power Supply System

The distributed power supply system concept is receiving increased attention as an alternative to the traditional centralized power supply. In a distributed power supply system, a front-end converter system rectifies and converts the mains voltage to an intermediate dc voltage of about 50 V. This intermediate voltage is then bussed to point-of-load converters that step it down to the working voltage, usually 5 V and ± 15 V. The purpose of this and a companion paper[1] is to describe the design of a very high efficiency, yet relatively small front-end converter.

A block diagram of a distributed power supply system is shown in Fig. 1. The front-end has two stages, the first of which is a power factor correction (PFC) unit. The PFC shapes the ac current to give near unity power factor, thus maximizing the real power that can be drawn from the mains. The unit described in [1] uses eight interleaved boost converters, each running at 25 kHz. The effect of interleaving is to give the low switching losses of 25 kHz operation and the low filtering requirements of 200 kHz operation. This PFC accommodates the universal input voltage range of 93-264 V r.m.s. and delivers 1.5 kW at a constant voltage of 390 V. It also incorporates a hold-up capacitor to which the input can be connected for up to 100 ms during power outages. During these outages the output voltage remains constant at 390 V because the hold-up capacitor is distinct from the output capacitor. The PFC achieves a minimum efficiency of 94% at low line.

As Fig. 1 shows, the PFC is followed by an isolation stage. This stage converts the 390 V to a 50 V bus voltage that is distributed to point-of-load converters. Because the input and output voltages of the isolation stage are constant, its design can be optimized. The converter topology, semiconductor devices, and other design variables can be chosen to take advantage of the constancy of the voltages, making this stage very efficient. The full power efficiency of the isolation stage prototype that this paper presents is better than 95.5% at 135 kHz with a power handling density of about 50 watts/in³. The overall efficiency of the complete front-end is therefore better than 90%.

Because of the constant input voltage, it is possible to run the isolation stage open loop, thus eliminating the stability problems associated with feedback regulation of the output voltage. The input voltage, and therefore the output voltage, is allowed to vary within $\pm 5\%$ of the nominal value. This variation, plus the ripple from the PFC and from the isolation stage, is corrected for by regulation capabilities of the point-of-load converters.

Fixed Input Voltage Operation

A transformer-coupled bridge topology with PWM control is used for the isolation stage. If the input voltage presented to this isolation stage is allowed to vary, say, over a two to one range, then the turns ratio N_p/N_s must be small enough for the output voltage to be maintained at its nominal value even at the lowest input voltage. At higher voltages, where the duty ratio is less than unity, the primary side switches therefore carry more current than they might otherwise have to, and the output rectifiers are stressed to a higher voltage. The result is increased MOSFET, rectifier, and transformer losses. This problem is particularly serious in full bridges controlled by the phase-shifted PWM technique, where, during the D' interval of operation, the load current freewheels in the primary side MOSFETs[2].

The problems described above are eased by keeping the input voltage to the isolation stage fixed. Not only does this reduce the dissipation in the semiconductor devices and the transformer, but it also allows the topology to be designed and operated to eliminate all the switching losses associated with the parasitic elements of the circuit.

The main causes of switching losses in PWM driven bridge topologies are the MOSFET output capacitors, the leakage inductance, and the rectifier capacitors. Unless measures are taken to prevent the dissipation of the energy stored in these elements each cycle, the efficiency of the converter will fall as the switching frequency is raised. The standard operation of a bridge topology recovers the energy in the leakage inductance but dissipates that in the capacitance of the semiconductor devices. The phase-shifted PWM control technique allows the energy in the MOSFET parasitic capacitors to be recovered, as well, but the energy in the rectifier capacitors is still lost[2]. The isolation stage discussed here recovers all three switching energies, and is therefore very efficient.

Topology and Theory of Operation

For this work, we used the half-bridge topology shown in Fig. 2 and operated it at a fixed duty ratio near unity (there is a small, fixed dead time between the two half cycles during which the MOSFETs Q_1 and Q_2 are switched). The capacitor shown across each semiconductor device represents its parasitic junction capacitance. Note that because $D \approx 1$, the load current never has to come solely out of the output filter for

